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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,660	04/12/2001	Luan C. Tran	MI22-1637	6625
21567	7590	12/28/2004	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			SCHILLINGER, LAURA M	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/834,660	Applicant(s) TRAN, LUAN C.	
	Examiner Laura M. Schillinger	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 21-30 and 63-80 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21-30 and 63-80 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/04/04</u> . | 6) <input type="checkbox"/> Other: _____  |

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## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21-30, 63-80 are rejected under 35 U.S.C. 102(e) as being anticipated by Liaw et al ('276).

In reference to claim 21, Liaw et al teaches a method comprising:

Forming two series of FETs over a substrate (Fig.1 (13 and 15 see also Col.s 2-3, lines: 65-5), one being isolated from adjacent devices by STI (Fig.3A (STI)), the other having active area widths greater than 1um (Fig.3A 12W) and , the one series being formed to have active area widths less than 1 um to achieve lower threshold voltages (TVs) than the other of the series (Fig.3A (12N) see also Col.4, lines: 55-65).

In reference to claim 22, Liaw et al teaches wherein the TVs for the 2 series of FETS are defined by a common channel implant (Col.3, lines: 30-45).

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In reference to claim 23, Liaw et al teaches wherein the threshold voltages for the two series of FETs are defined by a common channel implant, the implant being the only channel implant which defines the TVs for the two series of FETs (Col.4, lines: 5-6).

In reference to claim 24, Liaw et al teaches wherein the TVs for the two series of FETs are defined by one or more common channel implants (Col.3, lines: 30-45).

In reference to claim 25, Liaw et al teaches wherein the TVs for the two series of FETs are defined by one or more common channel implants, the common channel implants being the only channel implants which define the TV for the two series of FETs (Col.3, lines: 30-45).

In reference to claim 26, Liaw et al teaches a method of forming two series of FETs over a substrate (Fig.1 NMOS and PMOS (13 and 15)), one being isolated from adjacent devices by STI (Fig.3 (STI)), and achieving different TVs by varying the active widths of the FETs in the series providing a first series of transistors having active area widths less than active area widths of a second series of transistors and wherein the threshold voltages of the transistors of the first series are less than the threshold voltages of the transistors of the second series, at least one series having active area widths less than one micron (Fig.4).

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In reference to claim 27, Liaw et al teaches wherein the TVs for the 2 series of FETS are defined by a common channel implant (Col.4, lines: 5-6).

In reference to claim 28, Liaw et al teaches wherein the threshold voltages for the two series of FETs are defined by a common channel implant, the implant being the only channel implant which defines the TVs for the two series of FETs (Col.3, lines: 30-45).

In reference to claim 29, Liaw et al teaches wherein the TVs for the two series of FETs are defined by one or more common channel implants (Col.3, lines: 30-45).

In reference to claim 30, Liaw et al teaches wherein the TVs for the two series of FETs are defined by one or more common channel implants, the common channel implants being the only channel implants which define the TV for the two series of FETs (Col.3, lines: 30-45).

In reference to claim 61, Liaw et al teaches wherein the transistors of the two series comprise transistors having a single geometry type (Fig.1 (13 and 15)).

In reference to claim 62, Liaw et al teaches wherein the transistors of the single geometry type comprise planar transistors (Fig.1 (13 and 15)).

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In reference to claim 63, further comprising performing a common channel implant within active areas of the transistors of the two series at the same moment in time (Col.3, lines: 30-45).

64. The semiconductor processing method of claim 21, further comprising performing a common channel implant within active areas of both of the series of the transistors at the same moment in time to define the different threshold voltages of the transistors of the two series(Col.3, lines: 30-45).

65. The semiconductor processing method of claim 64, wherein the common channel implant is the only channel implant which defines the different threshold voltages of the transistors of the two series(Col.3, lines: 30-45).

66. Liaw teaches the semiconductor processing method of claim 21, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time(Col.3, lines: 30-45).

67. Liaw teaches the semiconductor processing method of claim 21, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time to simultaneously define the different threshold voltages of the transistors of the two series(Col.3, lines: 30-45 and Fig.4).

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68. Liaw teaches the semiconductor processing method of claim 67, wherein the implanting of the impurity is the only implant which defines the different threshold voltages of the transistors of the two series (Col.3, lines: 30-45 and Fig.4).

In reference to claim 69, Liaw et al teaches wherein the common channel implant comprises implanting a single type of impurity (boron-Col.3, lines: 30-45).

In reference to claim 70, Liaw et al teaches wherein the common channel implant comprises implanting a single type of impurity to define the different  $T_v$ s of the transistors of the two series (Col.4, lines 4-6).

73. Liaw teaches the semiconductor processing method of claim 26, further comprising performing a common channel implant within active areas of the transistors of the two series at the same moment in time (Col.3, lines: 30-45).

74. Liaw teaches the semiconductor processing method of claim 26, further comprising performing a common channel implant within active areas of both of the series of the transistors at the same moment in time to define the different threshold voltages of the transistors of the two series (Col.3, lines: 30-45).

75. Liaw teaches the semiconductor processing method of claim 74, wherein the common channel implant is the only channel implant which defines the different threshold voltages of the transistors of the two series (Col.3, lines: 30-45 and Fig.4).

76. Liaw teaches the semiconductor processing method of claim 26, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time (Col.3, lines: 30-45).

77. Liaw teaches the semiconductor processing method of claim 26, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time to simultaneously define the different threshold voltages of the transistors of the two series (Col.3, lines: 30-45 and Fig.4).

78. Liaw teaches the semiconductor processing method of claim 77, wherein the implanting of the impurity is the only implant which defines the different threshold voltages of the transistors of the two series (Col.3, lines: 30-45).

In reference to claim 79, Liaw et al teaches wherein the common channel implant comprises implanting a single type of impurity (boron-Col.3, lines: 30-45).

In reference to claim 80, Liaw et al teaches wherein the common channel implant comprises implanting a single type of impurity to define the different  $T_v$ s of the transistors of the two series (Col.4, lines 4-6).

In reference to claim 81, Liaw et al teaches wherein the active area widths individually correspond to a dimension of an active area of respective FET (12N and 12W) between plural STI regions (STI) immediately adjacent to opposing sides of the active are of the respective FET (12N and 12W) (Fig.3A)

In reference to claim 82, Liaw et al teaches wherein the active area widths individually correspond to a dimension of an active area of respective FET (12N and 12W) between plural STI regions (STI) immediately adjacent to opposing sides of the active are of the respective FET (12N and 12W) (Fig.3A)

### *Response to Arguments*

Applicant's arguments filed 10/04/04 have been fully considered but they are not persuasive.

With respect to claim 21, Applicant argues that Liaw fails to teach an active area width having less than 1 micron, wherein the threshold voltage is smaller than the wider active area widths. Applicant specifically refers to the Table on Col.4 to support this assertion. However, such an assertion is not supported by the Table found on Col.4 because the Table specifically shows having a smaller active area width corresponding to a smaller threshold voltage. In order to reduce confusion between the channel length and width, Applicant should refer to Fig.4 which draws a linear curve for each line of Table 4. As shown by the triangular and squared lines on Fig.4, as the channel width decreases, so does the threshold voltage.

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With respect to claim 22, Applicant argues that the dimensions taught by Liaw refer only to NMOS and not PMOS devices with respect to the boron implantation, Applicant requested clarification of any rejection of claim 22. The Examiner takes the position that when the boron is implanted into the channels, it modifies the threshold voltage and therefore “defines” the series of FETs. The term “define” is given its broadest reasonable interpretation by the Examiner and is based in part by the language of claims 23-25 which tend to infer that the aspect of the device being defined by the implantation is the threshold voltage.

With respect to claim 23, the above reasoning applies, that is that the boron implant modifies the threshold voltage and is therefore is the “defining” channel implant for the devices.

With respect to claim 24-25, the same reasoning again applies. Applicant may be inferring that one series of FET must be a PMOS transistor, and therefore the lack of boron implantation would negate the Examiner’s rejection. However, such an interpretation is not required by the Applicant’s claim language, as demonstrated in Fig. 4 there are multiple “series” of FETs taught with varying widths and varying dopants. Giving its broadest reasonable interpretation the two series could be any combination of a plurality of FETs with common characteristics.

With respect to claim 30, see the above remarks.

With respect to amended claim 26, as cited above, please refer to Fig. 4 as explained for claim 21 to see the small widths having small threshold voltages.

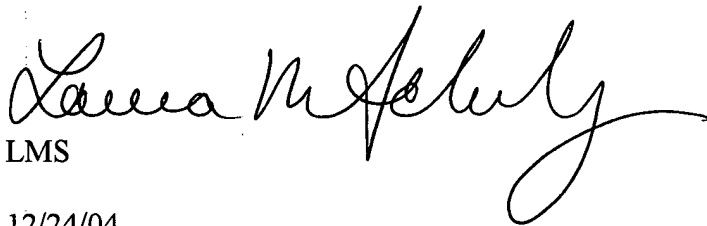
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*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
LMS

12/24/04